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RESEARCH INTERESTS	Nanoelectronic devices and architectures, particularly quantum-dot cellular automata (QCA); defect and fault tolerant design and modeling; high performance computing systems; computer-aided design and electronic design automation	
EDUCATION	University of Notre Dame , Notre Dame, Indiana <ul style="list-style-type: none"> • Ph.D, Computer Science and Engineering, 2009 • M.S., Computer Science and Engineering, 2005 • B.S. (<i>Cum Laude</i>), Computer Engineering, 2002 	
PROFESSIONAL EXPERIENCE	University of Notre Dame , Notre Dame, Indiana <ul style="list-style-type: none"> • Post-doctoral Research Associate August 2009 to Present • Graduate Research Assistant July 2002 to August 2009 Delphi (Delco Electronics) Automotive Systems , Kokomo, Indiana <ul style="list-style-type: none"> • Integrated Circuit Design Intern Summer 2001 • Software Development Intern Summer 2000 	
TEACHING EXPERIENCE	University of Notre Dame <ul style="list-style-type: none"> • Instructor: Computer Architecture II Spring Semester 2006, 2007 • Teaching Assistant: Computer Architecture II Spring Semester 2004 • Teaching Assistant: Computer Architecture I Fall Semester 2003, 2004 • Undergraduate Teaching Assistant: Discrete Math Spring Semester 2001 	
PAPERS UNDER REVIEW (1)	T.J. Dysart and P.M. Kogge, "Reliability Impact of N-Modular Redundancy in Quantum-Dot Cellular Automata," Submitted to <i>IEEE Trans. on Nanotechnology</i>	
JOURNAL PUBLICATIONS (3)	T.J. Dysart and P.M. Kogge, "Organizing Wires for Reliability in Magnetic QCA," Accepted for publication in <i>ACM Journal on Emerging Technologies in Computing Systems</i> T.J. Dysart and P.M. Kogge, "Analyzing the Inherent Reliability of Moderately Sized Magnetic and Electrostatic QCA Circuits via Probabilistic Transfer Matrices," <i>IEEE Trans. on VLSI</i> , Vol. 17, Num. 4, pp. 507-516, April 2009	

K. Walus, **T.J. Dysart**, G.A. Jullien, A.R. Budiman, "QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata," *IEEE Transactions on Nanotechnology*, Vol. 3, Num. 1, pp. 26-31, March 2004

REFEREED
CONFERENCE
AND WORKSHOP
PUBLICATIONS
(11)

T.J. Dysart and P.M. Kogge, "System Reliabilities when Using Triple Modular Redundancy in Quantum-Dot Cellular Automata," In *Proceedings of the 23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 72-80, Oct. 2008

T.J. Dysart, D.J. Lohmer, P.M. Kogge, "Using Geometric Analysis to Estimate the Yield of Molecular QCA Memory Structures," In *Proceedings of the 1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems*, pp. 45-48, Sept. 2008

T.J. Dysart and P.M. Kogge, "Comparing the Reliability of PLA and Custom Logic Implementations of a QCA Adder," In *Proceedings of the 1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems*, pp. 53-56, Sept. 2008

T.J. Dysart and P.M. Kogge, "Probabilistic Analysis of a Molecular Quantum Dot Cellular Automata Adder," In *Proceedings of the 22nd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 478-486, Sept. 2007

T.J. Dysart and P.M. Kogge, "Probabilistic Analysis of a Quantum-Dot Cellular Automata Multiplier Implemented in Different Technologies," In *Proceedings of the 4th Non-Silicon Computing Workshop* held in conjunction with the 34th International Symposium on Computer Architecture and the Federated Computing Research Conference 2007, pp. 41-48, June 2007

T.J. Dysart, P.M. Kogge, C.S. Lent, and M. Liu, "An Analysis of Missing Cell Defects in Quantum-Dot Cellular Automata," In *Proceedings of the 1st IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH)* held in conjunction with the VLSI Test Symposium, pp. 3.1-3.8, May 2005

S.E. Frost, **T.J. Dysart**, P.M. Kogge, and C.S. Lent, "Carbon Nanotubes for Quantum-Dot Cellular Automata Clocking," In *Proceedings of the 4th IEEE Conference on Nanotechnology*, pp. 171-173, Aug. 2004

D.A. Antonelli, D.Z. Chen, **T.J. Dysart**, X.S. Hu, A.B. Kahng, P.M. Kogge, R.C. Murphy, and M.T. Niemier, "Quantum Dot Cellular Automata Circuit Partitioning: Problem Modeling and Solutions," In *Proceedings of the 41st Design Automation Conference*, pp. 363-368, June 2004

T.J. Dysart, B.J. Moore, L. Schaelicke, P.M. Kogge, "Cache Implications of Aggressively Pipelined High Performance Microprocessors," In *Proceedings of the 4th IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 123-132, Mar. 2004

T.J. Dysart and P.M. Kogge, "Strategy and Prototype Tool for Doing Fault Modeling in a Nanotechnology," In *Proceedings of the 3rd IEEE Conference on Nanotechnology*, Vol. 2, pp. 356-359, Aug. 2003

K. Walus, **T.J. Dysart**, G.A. Jullien, A.R. Budiman, "QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata," In *Proceedings of the 2nd International Workshop on Quantum Dots for Quantum Computing and Classical Size Effect Circuits*, pp. 22-23, Aug. 2003, *Note: Refereed Abstract*

OTHER
PUBLICATIONS
(4)

T.J. Dysart, "It's All About the Signal Routing: Understanding Reliability in QCA Circuits and Systems," Ph.D. Dissertation, 2009

T.J. Dysart, D.J. Lohmer, P.M. Kogge, "Missing Cell Patterns Causing Circuit Failures In Densely Packed Molecular QCA Wires," Technical Report 2008-08, Dept. of Computer Science and Engineering, University of Notre Dame

T.J. Dysart, "Defect Properties and Design Tools for Quantum Dot Cellular Automata," Master's Thesis, 2005

T.J. Dysart and P.M. Kogge, "XML Based File Format for QCADesigner," Technical Report 2004-26, Dept. of Computer Science and Engineering, University of Notre Dame

INVITED TALKS

It's All About the Signal Routing: Understanding the Reliability of QCA Circuits and Systems, 1st International Workshop on Quantum-Dot Cellular Automata, Vancouver, B.C., Aug. 2009

UNDER-
GRADUATE
PROJECTS
SUPERVISED

Jorge Vendries Summer and Fall Semester 2008
• Parallelization of a statistical mechanical QCA simulator

Daniel Lohmer Spring Semester 2008
• Geometric analysis of QCA wires
• Workshop paper published in 2008

Jared Sylvester Academic Year 2004-2005
• Logic reduction in QCA

Dominic Antonelli Summer 2003
• Digital logic simulators for QCA circuits
• Created a stand-alone version and one integrated with QCADesigner

HONORS AND AWARDS	<p>Upsilon Pi Epsilon (Computer Science and Engineering Honor Society), Inducted 2004 (Inaugural induction)</p> <p>Eta Kappa Nu (Electrical and Computer Engineering Honor Society), Inducted 2002</p>
SERVICE	<p>Reviewer for the following:</p> <ul style="list-style-type: none"> • ACM Journal on Emerging Technologies in Computing Systems • Integration, the VLSI Journal (Publisher: Elsevier) • IEEE Transactions on CAD of Integrated Circuits and Systems • IEEE Transactions on Nanotechnology • IEEE Transactions on VLSI • Institution of Engineering and Technology (IET) Electronics Letters • Microelectronics Journal (Publisher: Elsevier)
PROFESSIONAL ORGANIZATIONS	<p>Association for Computing Machinery (ACM)</p> <ul style="list-style-type: none"> • SIGARCH <p>Institute for Electrical and Electronics Engineers (IEEE)</p> <ul style="list-style-type: none"> • IEEE-Computer Society
WORKSHOPS ATTENDED	<p>Kaneb Center for Teaching and Learning, University of Notre Dame</p> <ul style="list-style-type: none"> • Effective Lecturing • What Makes a Great Lecture 'Great' • Early Semester Evaluations • Preparing for an Academic Career in Physics, Math and Engineering <p>Office of Research, University of Notre Dame</p> <ul style="list-style-type: none"> • Writing Successful Grants
LAST UPDATED	August 18, 2009