

CONTACT  
INFORMATION

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RESEARCH  
INTERESTS

Nanoelectronic devices and architectures, particularly quantum-dot cellular automata (QCA); defect and fault tolerant design and modeling; high performance computing systems; computer-aided design and electronic design automation

## EDUCATION

**University of Notre Dame**, Notre Dame, Indiana

Ph.D, Computer Science and Engineering, August 2009

- Dissertation Title: It's All About the Signal Routing: Understanding the Reliability of QCA Circuits and Systems
- Advisor: Dr. Peter M. Kogge

M.S., Computer Science and Engineering, 2005

- Thesis Title: Defect Properties and Design Tools for Quantum Dot Cellular Automata
- Advisor: Dr. Peter M. Kogge

B.S. (*Cum Laude*), Computer Engineering, 2002

PROFESSIONAL  
EXPERIENCE

**University of Notre Dame**, Notre Dame, Indiana

*Post-doctoral Research Associate*

*August 2009 to Present*

- **Topics below subject to change.**
- Architectures for QCA circuits
- Energy modeling for high-performance computing systems
- Communication modeling for high-performance computing systems

*Graduate Research Assistant*

*July 2002 to August 2009*

- Development of simulation tools for QCA circuits
- Reliability studies of defective QCA interconnect
- Analytic reliability modeling of QCA circuits and systems

**Delphi (Delco Electronics) Automotive Systems**, Kokomo, Indiana

*Integrated Circuit Design Intern*

*Summer 2001*

- Modified circuit designs to be fabricated using a new process
- Performed various tests on circuits from a new fabrication process

*Software Development Intern*

*Summer 2000*

- Developed a dynamic link library (DLL) for use with controller-area network (CAN) based devices

TEACHING  
EXPERIENCE

**University of Notre Dame**, Notre Dame, Indiana

*Instructor: Computer Architecture II* *Spring Semester 2006, 2007*

- Junior level course required for computer engineering majors
- Approximately 15 students per term
- 4 credit course (3 lecture, 1 lab)
- Supervised one teaching assistant each semester

*Teaching Assistant: Computer Architecture II* *Spring Semester 2004*

- Taught all lab sections (bi-weekly)
- Graded all homework and lab assignments

*Teaching Assistant: Computer Architecture I* *Fall Semester 2003, 2004*

- Junior level course required for computer science and engineering majors
- Approximately 40 students per term
- 4 credit course (3 lecture, 1 lab)
- Shared teaching lab sessions and grading responsibilities with a second graduate teaching assistant

*Undergraduate Teaching Assistant: Discrete Math* *Spring Semester 2001*

- Sophomore level course required for computer science and engineering majors
- Approximately 40 students
- Held office hours for students in course

PAPERS UNDER  
REVIEW

**T.J. Dysart** and P.M. Kogge, "Reliability Impact of N-Modular Redundancy in Quantum-Dot Cellular Automata," Submitted to *IEEE Trans. on Nanotechnology*

JOURNAL  
PUBLICATIONS  
(3)

**T.J. Dysart** and P.M. Kogge, "Organizing Wires for Reliability in Magnetic QCA," Accepted for publication in *ACM Journal on Emerging Technologies in Computing Systems*

**T.J. Dysart** and P.M. Kogge, "Analyzing the Inherent Reliability of Moderately Sized Magnetic and Electrostatic QCA Circuits via Probabilistic Transfer Matrices," *IEEE Trans. on VLSI*, Vol. 17, Num. 4, pp. 507-516, April 2009

K. Walus, **T.J. Dysart**, G.A. Jullien, A.R. Budiman, "QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata," *IEEE Trans. on Nanotechnology*, Vol. 3, Num. 1, pp. 26-31, March 2004

**T.J. Dysart** and P.M. Kogge, "System Reliabilities when Using Triple Modular Redundancy in Quantum-Dot Cellular Automata," In *Proceedings of the 23<sup>rd</sup> IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 72-80, Oct. 2008

**T.J. Dysart**, D.J. Lohmer, P.M. Kogge, "Using Geometric Analysis to Estimate the Yield of Molecular QCA Memory Structures," In *Proceedings of the 1<sup>st</sup> IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems*, pp. 45-48, Sept. 2008

**T.J. Dysart** and P.M. Kogge, "Comparing the Reliability of PLA and Custom Logic Implementations of a QCA Adder," In *Proceedings of the 1<sup>st</sup> IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems*, pp. 53-56, Sept. 2008

**T.J. Dysart** and P.M. Kogge, "Probabilistic Analysis of a Molecular Quantum Dot Cellular Automata Adder," In *Proceedings of the 22<sup>nd</sup> IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 478-486, Sept. 2007

**T.J. Dysart** and P.M. Kogge, "Probabilistic Analysis of a Quantum-Dot Cellular Automata Multiplier Implemented in Different Technologies," In *Proceedings of the 4<sup>th</sup> Non-Silicon Computing Workshop* held in conjunction with the 34<sup>th</sup> International Symposium on Computer Architecture and the Federated Computing Research Conference 2007, pp. 41-48, June 2007

**T.J. Dysart**, P.M. Kogge, C.S. Lent, and M. Liu, "An Analysis of Missing Cell Defects in Quantum-Dot Cellular Automata," In *Proceedings of the 1<sup>st</sup> IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH)* held in conjunction with the VLSI Test Symposium, pp. 3.1-3.8, May 2005

S.E. Frost, **T.J. Dysart**, P.M. Kogge, and C.S. Lent, "Carbon Nanotubes for Quantum-Dot Cellular Automata Clocking," In *Proceedings of the 4<sup>th</sup> IEEE Conference on Nanotechnology*, pp. 171-173, Aug. 2004

D.A. Antonelli, D.Z. Chen, **T.J. Dysart**, X.S. Hu, A.B. Kahng, P.M. Kogge, R.C. Murphy, and M.T. Niemier, "Quantum Dot Cellular Automata Circuit Partitioning: Problem Modeling and Solutions," In *Proceedings of the 41<sup>st</sup> Design Automation Conference*, pp. 363-368, June 2004

**T.J. Dysart**, B.J. Moore, L. Schaelicke, P.M. Kogge, "Cache Implications of Aggressively Pipelined High Performance Microprocessors," In *Proceedings of the 4<sup>th</sup> IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 123-132, Mar. 2004

**T.J. Dysart** and P.M. Kogge, "Strategy and Prototype Tool for Doing Fault Modeling in a Nanotechnology," In *Proceedings of the 3<sup>rd</sup> IEEE Conference on Nanotechnology*, Vol. 2, pp. 356-359, Aug. 2003

K. Walus, **T.J. Dysart**, G.A. Jullien, A.R. Budiman, "QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata," In *Proceedings of the 2<sup>nd</sup> International Workshop on Quantum Dots for Quantum Computing and Classical Size Effect Circuits*, pp. 22-23, Aug. 2003, *Note: Refereed Abstract*

OTHER  
PUBLICATIONS  
(4)

**T.J. Dysart**, "It's All About the Signal Routing: Understanding Reliability in QCA Circuits and Systems," Ph.D. Dissertation, 2009

**T.J. Dysart**, D.J. Lohmer, P.M. Kogge, "Missing Cell Patterns Causing Circuit Failures In Densely Packed Molecular QCA Wires," Technical Report 2008-08, Dept. of Computer Science and Engineering, University of Notre Dame

**T.J. Dysart**, "Defect Properties and Design Tools for Quantum Dot Cellular Automata," Master's Thesis, 2005

**T.J. Dysart** and P.M. Kogge, "XML Based File Format for QCADesigner," Technical Report 2004-26, Dept. of Computer Science and Engineering, University of Notre Dame

INVITED TALKS

*It's All About the Signal Routing: Understanding the Reliability of QCA Circuits and Systems*, 1<sup>st</sup> International Workshop on Quantum-Dot Cellular Automata, Vancouver, B.C., Aug. 2009

UNDER-  
GRADUATE  
PROJECTS  
SUPERVISED

*Jorge Vendries* *Summer and Fall Semester 2008*  
• Parallelization of a statistical mechanical QCA simulator

*Daniel Lohmer* *Spring Semester 2008*  
• Geometric analysis of QCA wires  
• Workshop paper published in 2008

*Jared Sylvester* *Academic Year 2004-2005*  
• Logic reduction in QCA

*Dominic Antonelli* *Summer 2003*  
• Digital logic simulators for QCA circuits  
• Created a stand-alone version and one integrated with QCADesigner

HONORS AND AWARDS	<p>Upsilon Pi Epsilon (Computer Science and Engineering Honor Society), Inducted 2004 (Inaugural induction)</p> <p>Eta Kappa Nu (Electrical and Computer Engineering Honor Society), Inducted 2002</p>
SERVICE	<p>Reviewer for the following:</p> <ul style="list-style-type: none"> <li>• ACM Journal on Emerging Technologies in Computing Systems</li> <li>• Integration, the VLSI Journal (Publisher: Elsevier)</li> <li>• IEEE Transactions on CAD of Integrated Circuits and Systems</li> <li>• IEEE Transactions on Nanotechnology</li> <li>• IEEE Transactions on VLSI</li> <li>• Institution of Engineering and Technology (IET) Electronics Letters</li> <li>• Microelectronics Journal (Publisher: Elsevier)</li> </ul>
PROFESSIONAL ORGANIZATIONS	<p>Association for Computing Machinery (ACM)</p> <ul style="list-style-type: none"> <li>• SIGARCH</li> </ul> <p>Institute for Electrical and Electronics Engineers (IEEE)</p> <ul style="list-style-type: none"> <li>• IEEE-Computer Society</li> </ul>
WORKSHOPS ATTENDED	<p>Kaneb Center for Teaching and Learning, University of Notre Dame</p> <ul style="list-style-type: none"> <li>• Effective Lecturing</li> <li>• What Makes a Great Lecture 'Great'</li> <li>• Early Semester Evaluations</li> <li>• Preparing for an Academic Career in Physics, Math and Engineering</li> </ul> <p>Office of Research, University of Notre Dame</p> <ul style="list-style-type: none"> <li>• Writing Successful Grants</li> </ul>
LAST UPDATED	August 18, 2009