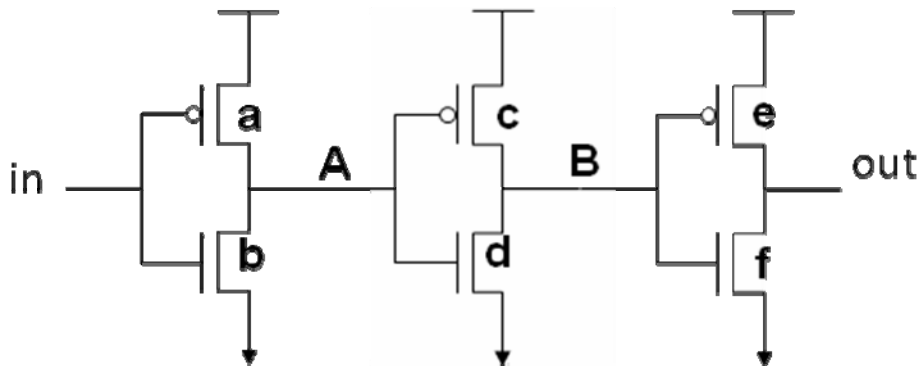


CSE 40462 VLSI Design
 Homework 5
 Due Friday Oct 2, 2009

1. Simulate the following three inverters using the UofU_TechLib_ami06 process library for two cases:
 - i) $a = c = e = W/L = 2.0 \mu\text{m}/0.6 \mu\text{m}$ and $b = d = f = W/L = 1.0 \mu\text{m}/0.6 \mu\text{m}$.

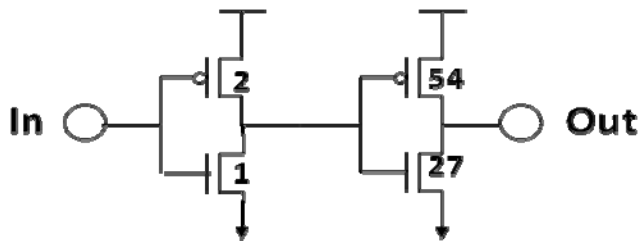


- ii) The same dimensions as (i) except $c = 1.0 \mu\text{m}/0.6 \mu\text{m}$.

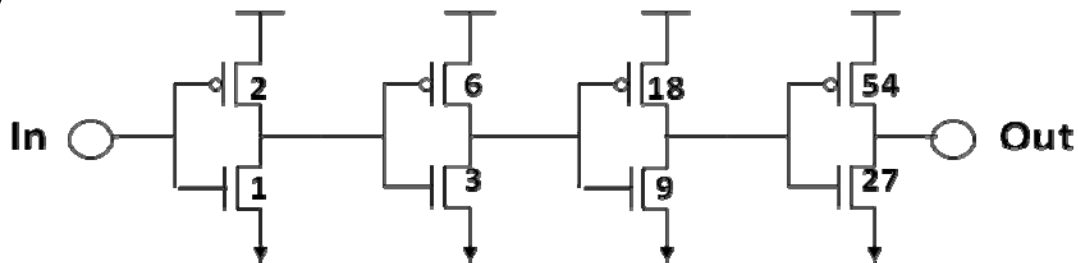
- a) What are the simulated propagation delays t_{pHL} , t_{pLH} , and t_p from node A to node B for each case?
- b) How does the simulated delay compare to the estimated delay using the estimated R and C values for the $0.6 \mu\text{m}$ process as given in class?
 Use $V_{DD} = 5\text{V}$ and a 10 ps rise and fall time on the input pulse.

2. Simulate the three cases we discussed in class using the UofU_TechLib_ami06 process library.

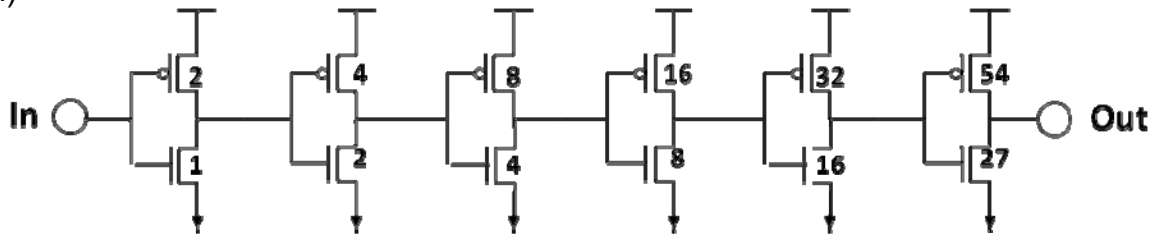
- i)



- ii)



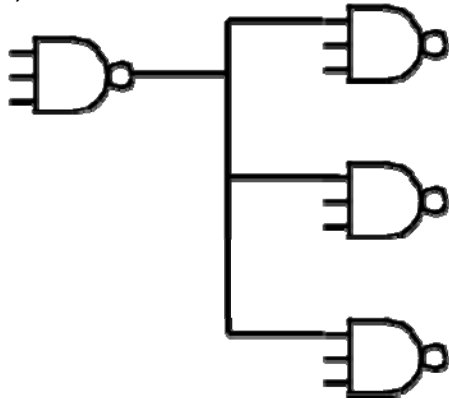
iii)



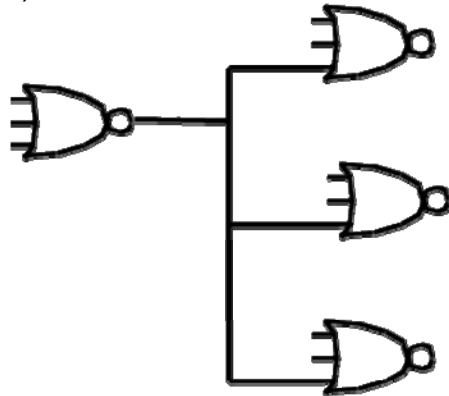
- What is the delay from In to Out in each case?
- How does the simulation delay compare to the estimated delays in class? Use the estimated R and C values for a 0.6 μm process as discussed in class.

3. For the following two logic stages, one with 3 input NAND and one with 3 input NOR gates:

i) NAND



ii) NOR



- If an inverter has a nmos transistor with W/L of 1 and a pmos transistor with W/L of 2, what are the sizes of the nmos transistors and pmos transistors in NAND and NOR gates for similar output drives (values of R_{eff})?
- What is the delay in the shown logic stages for the NAND circuit and the NOR circuit? (Give the answer in terms of the R and C for the inverter nmos transistor channel and gate respectively.) For the NAND gate, assume that the nmos transistor closest to the output is switched while for the NOR gate, assume that the pmos transistor closest to the output is switched.
- Which is faster NAND or NOR? Why?

4. Develop (and just write down – no simulation yet) a behavioral model for a 2 input exclusive or gate using just “&”, “|”, and “~”. Thus using this module develop a structural module for an 8 input parity generator – i.e. there are 8 data inputs which are combined by 3 levels of xors to compute the odd parity of the data bits. This parity should be the output of the module.