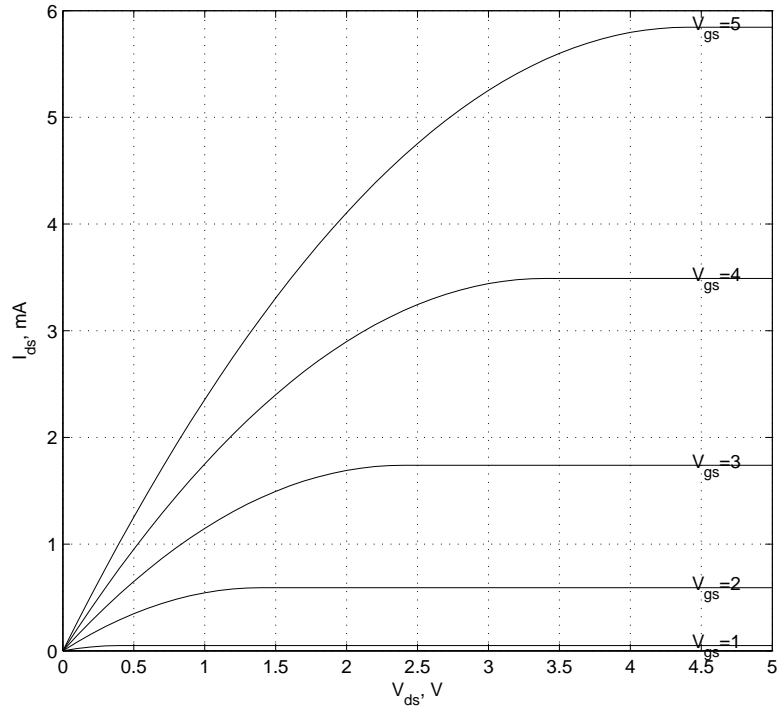


CSE 40462 VLSI Design
Homework 4: MOS Devices
 See Class web site for due date

1. Consider the device in the IV plot shown below:



- (a) Does this transistor exhibit significant effects of velocity saturation? Explain.
- (b) Determine V_t
- (c) Determine β
- (d) Determine the channel length modulation factor, λ
- (e) If both the width and length of the transistor were doubled, estimate the value of the current between the source and drain when $V_{gs} = V_{ds} = 4V$. What is the region of operation for the transistor under these bias conditions?

2. From Rabaey, *Digital Integrated Circuits*, problem 2.4:

Determine the mode of operation (cutoff, linear, or saturation) and the drain current I_{ds} for each of the biasing configurations below for an NMOS transistor. Use the following transistor data: $\beta = 60 \mu A/V^2$, $V_t = 0.7 V$, $\lambda = 0.1 V^{-1}$.

- (a) $V_{gs} = 3.3 V$, $V_{ds} = 3.3 V$
- (b) $V_{gs} = 3.3 V$, $V_{ds} = 2.2 V$
- (c) $V_{gs} = 0.6 V$, $V_{ds} = 0.1 V$

Determine the mode of operation (cutoff, linear, or saturation) and the drain current I_{ds} for each of the biasing configurations below for an PMOS transistor. Use the following transistor data: $\beta = 20 \mu\text{A}/\text{V}^2$, $V_t = -0.8 \text{ V}$, $\lambda = 0.1 \text{ V}^{-1}$.

(a) $V_{gs} = -0.5 \text{ V}$, $V_{ds} = -1.5 \text{ V}$

(b) $V_{gs} = -3.3 \text{ V}$, $V_{ds} = -2.6 \text{ V}$

(c) $V_{gs} = -3.3 \text{ V}$, $V_{ds} = -0.5 \text{ V}$

3. From Rabaey, *Digital Integrated Circuits*, problem 2.9:

The data points were measured for an NMOS transistor, with $\beta = 20 \mu\text{A}/\text{V}^2$. Determine the values of V_t , W/L and λ

V_{gs} (V)	V_{ds} (V)	I_d (μA)
3	5	1210
5	5	4410
5	10	5292

4. Weste & Harris 2.21

5. Weste & Harris 2.22