 **CSE 221: Logic Design, Spring 2004**

**CHAPTER 9:**  
**Memory**

### Overview

- Random-Access Memory
  - Read/Write Operations
  - Timing Waveforms
  - SRAM Vs. DRAM
- RAM ICs
  - RAM cell
  - RAM bit slice
  - Coincident Selection
- Arrays of RAM ICs

Apr-22-04 PJF - 2

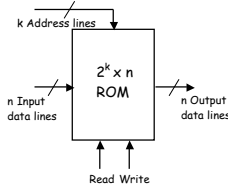
### Random-Access Memory (RAM)

- Memory cells are accessed (for reading or writing) with the **access time being the same** regardless where the cells are located.
- This is in contrast to **serial memory** (ex. magnetic disk or tape), where it takes different time to access data depending on where the data is relative to the current physical location.

Apr-22-04 PJF - 3

### RAM block diagram

- A **word** is a collection of bits that act as a unit
- Each word has a corresponding **address location**



Communications between the memory and its environment is achieved by:

- Input/Output data lines
- Address lines
- Control signals

word size = n  
# of words =  $2^k$   
address locations =  $0 \dots 2^k - 1$

Apr-22-04 PJF - 4

### Example: A 1024 x 16 RAM

Memory address		Memory contents
Binary	Decimal	
000000000	0	10110101 01011100
000000001	1	10101011 10001001
000000010	2	00001101 01000110
⋮	⋮	⋮
⋮	⋮	⋮
111111101	1021	10011101 00010101
111111110	1022	00001101 00011110
111111111	1023	11011110 00100100

There are 1024 memory locations ( 0 - 1023 ), each of which can hold 16-bit words.

Apr-22-04 PJF - 5

### Memory Control

□ **TABLE 9-1**  
**Control Inputs to a Memory Chip**

Chip select CS	Read/Write R/W	Memory operation
0		None
1	0	Write to selected word
1	1	Read from selected word

Apr-22-04 PJF - 6

### Read and Write operations

- **Write:** transfer data into the RAM
  1. Load the address lines
  2. Load the data lines
  3. Activate the write operation (write=1)
- **Read:** transfer from RAM to output data lines
  1. Load address lines
  2. Activate the read operation (read=1)

Apr-22-04 PJF - 7

### Access and Write Cycle Time

- **Access time (r)** = maximum time required from the loading of the address lines to the appearance of the data on the Output data lines.
- **Write cycle time (w)** = maximum time required from the loading of the address lines to completing all operations associated with storing a word.
- Typically,  $r < w$ .

Apr-22-04 PJF - 8

### Timing Waveforms

- We must synchronize the various memory operations with the CPU clock.
- Question: Let the CPU clock period to be  $p$  ns, RAM access time to be  $r$  ns, and RAM write cycle time to be  $w$  ns. Assume that  $p < r$  and  $p < w$ . What is the minimum # of cycles that the CPU has to wait for a memory operation to complete?
- Answer:  $\lceil \max\{r,w\}/p \rceil$

Apr-22-04 PJF - 9

### Timing Waveforms (Example)

Apr-22-04 PJF - 10

### Types of RAM

Static (SRAM)	Dynamic (DRAM)
1. Faster	Slower
2. More expensive	Less expensive
3. Smaller	Larger
Why?	
4. Uses latches (logic)	Electric charges is stored on capacitor, accessed inside the chip by nMOS transistors.
5. No refreshing is required	Capacitors must be recharged

Apr-22-04 PJF - 11

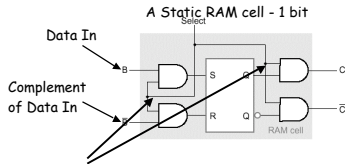
### RAM Integrated Circuits

- Memory consists of:
  - RAM chips
  - Read/Write logic
  - Selection logic

Apr-22-04 PJF - 12

## RAM Cell

- Typically, it is designed as an electronic cct. We are only concerned with how it operates, so we will view it as a logic cct.



When Select is 0,  $S = 0, R = 0$   
 S-R Latch is in No Change State  
 Outputs C and C-bar are both 0  
 When Select is 1, the Data in and its complement get latched into the memory cell

Recall...

(b) SR Flip-Flop			
S	R	Q (r 1)	Operation
0	0	Q(0)	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

Apr-22-04

## RAM Bit Slice

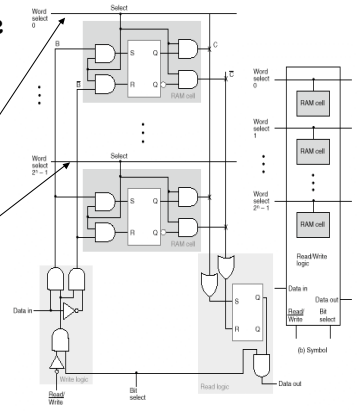
All circuitry associated with a single bit position of a set of RAM words (ie. a RAM column)

0110	1001
0100	0011
1110	1011
0111	1000

4 x 8 RAM  
 4 memory locations,  
 8 - bits each

If Bit select = 0, RAM remains unchanged.  
 If Read/Write = 0, then Data In is loaded to the selected RAM cell.  
 Read occurs regardless of the value of Read/Write.

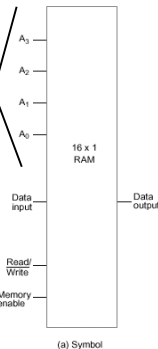
Apr-22-04



## A 16 x 1 RAM Chip

16 memory locations,  
 1 bit each

$2^k$  locations with k select lines  
 $2^k=16, k = 4$



(a) Symbol

Apr-22-04

PJF - 15

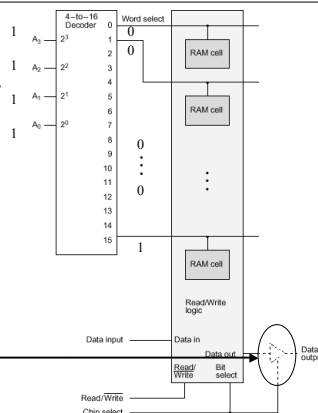
## A 16 x 1 RAM Chip

Decoder controls  
 Address Selections

Address decoder enables the RAM cell for the 1-bit word selected and disables all others

Tri - State Buffer,  
 When chip select is 0 there is no connecting path between the 16x1 RAM and the data output line

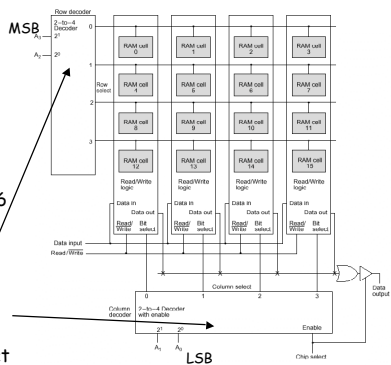
Apr-22-04



## Coincident Selection

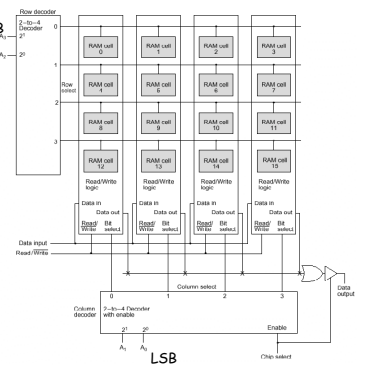
Using a 4 x 4 RAM CELL Array to implement a 16 x 1 RAM  
 → Break the single 4-to-16 DEC to two 2-to-4 DEC.

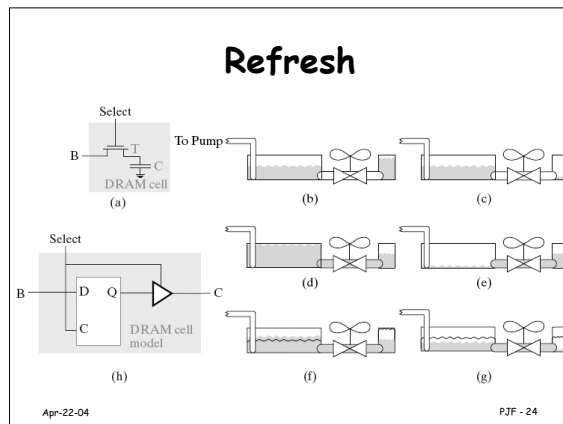
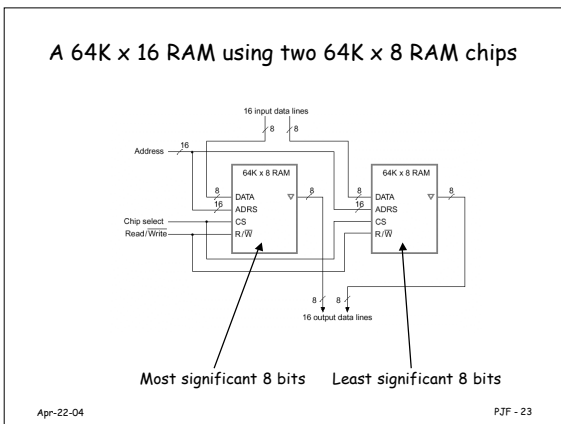
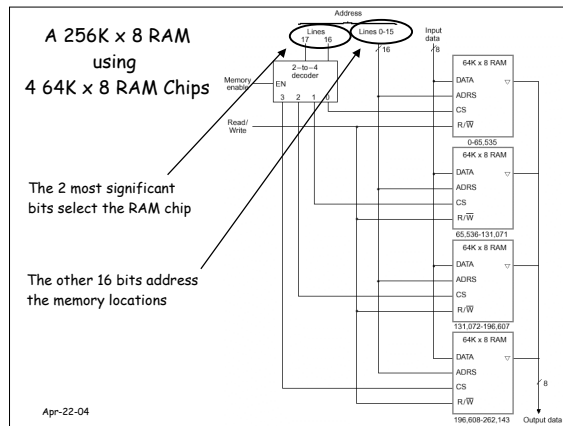
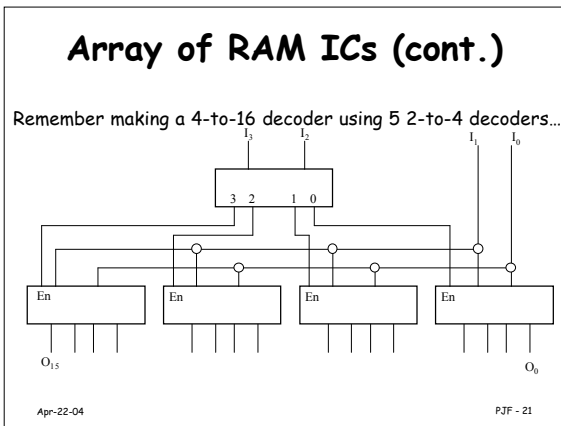
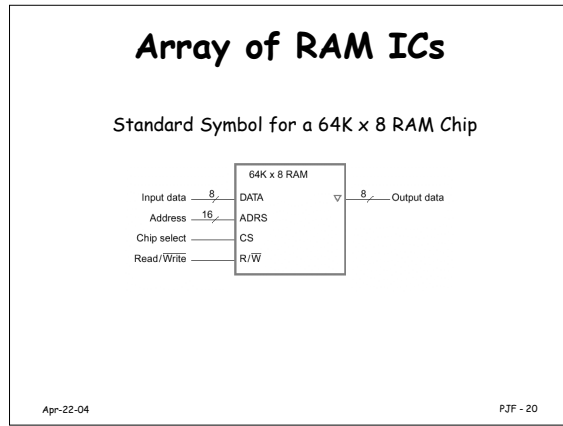
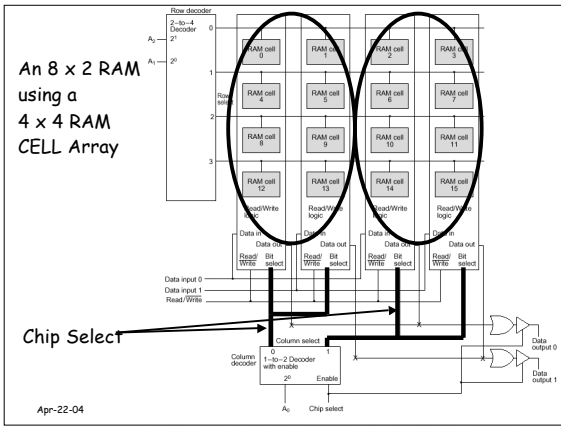
Row Select  
 Column Select



## Coincident Selection

As k increases, savings in H/W are VERY considerable!  
 This occurs due to the DEC size reduction  
 → Smaller DEC means fewer AND gates  
 (recall that a k-to-m DEC requires  $m=2^k$ )





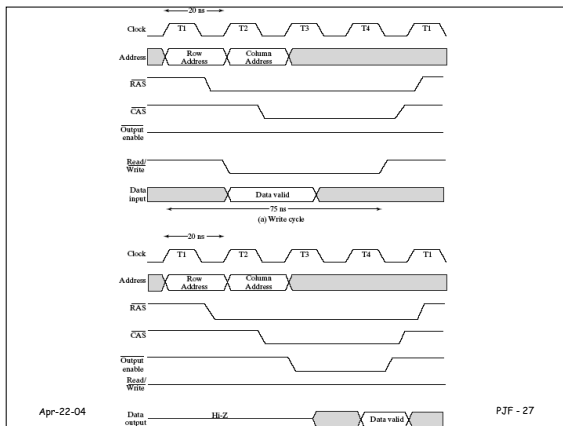
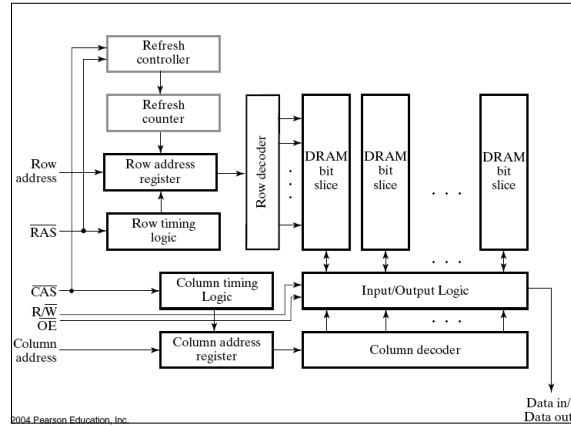
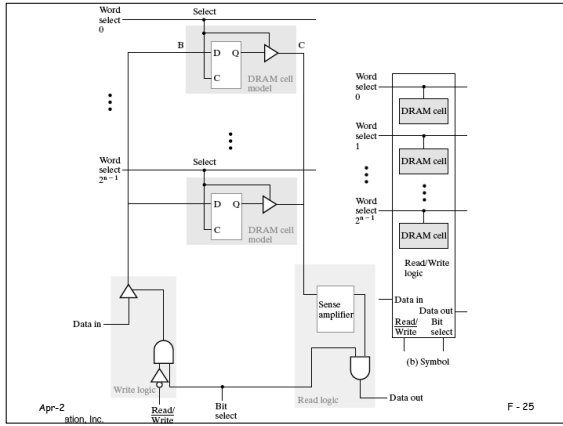


TABLE 9-2  
DRAM Types

Type	Abbreviation	Description
Fast Page Mode DRAM	FPM DRAM	Takes advantage of the fact that, when a row is accessed, all of the row values are available to be read out. By changing the column address, data from different addresses can be read out without reapplying the row address and waiting for the delay associated with reading out the row cells to pass if the row portion of the addresses match.
Extended Data Output DRAM	EDO DRAM	Extends the length of time that the DRAM holds the data values on its output, permitting the CPU to perform other tasks during the access since it knows the data will still be available.
Synchronous DRAM	SDRAM	Operates with a clock rather than being asynchronous. This permits a tighter interaction between memory and CPU, since the CPU knows exactly when the data will be available. SDRAM also takes advantage of the row value availability and divides memory into distinct banks, permitting overlapped accesses.
Double Data Rate Synchronous DRAM	DDR SDRAM	The same as SDRAM except that data output is provided on both the negative and the positive clock edges.
Rambus DRAM	RDRAM	A proprietary technology that provides very high memory access rates using a relatively narrow bus.
Error-Correcting Code	ECC	May be applied to most of the DRAM types above to correct single bit data errors and often detect double errors.

Apr-22-04 PJF - 28

