

Introduction to NAND, NOR and XOR Gates; Design of Multiple-Switch Lamp Controls

Introduction

In the previous experiment we saw how any combinational logic function may be realized using AND, OR, and NOT gates. In this experiment we verify that the NAND gate is a universal building block. That is, the operation is functionally complete, in that any combinational logic function may be realized solely with NAND gates. We also verify that the NOR gate, which is the dual of the NAND, is also a universal building block. Finally, we investigate the use of the Exclusive OR (XOR) operation in the design of a two-switch lamp control.

This is a two-week laboratory with parts MG2 and HD2 denoting Mentor Graphics and Hardware, respectively. Part MG2, the schematic creation and simulation using Mentor Graphics Design Architect and QuickSim, should be completed during the first week. Part HD2 will utilize the IDL-800 Logic Lab units during the second week.

Part MG2 (First Week)

In the first laboratory session you learned how to create a simple circuit using the Design Architect. This experiment will direct you step by step through the setup and simulation of a more complicated circuit to verify that each of the operators NAND and NOR is functionally complete, so that each corresponding gate is a universal building block. With that background, you are requested to perform your own design, setup and simulation of **a two-switch lamp control, contrasting a circuit of four NAND gates with the use of a single XOR gate.**

Part MG2A. NAND and NOR Gate Simulation

The schematic sheet labeled Experiment MG2A on Page 8 shows two inputs, A and B, driving three groups of gates. The first group implements the basic Boolean operations of AND, OR and NOT. The second group performs these same operations using solely NAND gates, and the third group does the same thing solely with NOR gates. Note that two methods are shown for generating NOT with both NAND and NOR gates. The simulated waveforms shown on Page 8 verify that the NAND and NOR gates are indeed universal building blocks. You are to replicate the schematic and waveform diagrams by following the steps outlined below. This procedure assumes that you are in the OpenWindows environment.

Note: (LMB, MMB, RMB) = (Left, Middle, Right) Mouse Button.

In the detailed procedures given below, we normally indicate only one method to initiate a

specific action. Keep in mind, however, that some actions such as *unselect all* can be initiated in as many as six different ways: function key, pull-down menu, pop-up menu, schematic palette, stroke with the middle mouse button, and keyboard command entry. Note that there is a multiple-level undo action for error recovery. The menus are context sensitive. Draw a question mark with the middle mouse button to see what strokes are available.

a) Schematic Creation with Design Architect

1. You should use a separate directory for your Mentor Graphics work. You may use the directory which you created in Laboratory MG1, or you can create a new one by typing **mkdir directory_name** For security reasons, please create all your directories under the Private directory. Otherwise change access rights of the directory you created. Go to the directory in which you intended to work on Mentor Graphics for cse221.
2. Type **dmgr &** to invoke the Design Manager. Start up Design Architect window. Maximize the window.
3. Click the LMB on [session_palette] *OPEN SHEET*. The name within brackets denotes the header of the palette on the right side of the DA window. In the resulting dialog window, type **MG2A** for the Component Name, and click OK (or press the Return key). A new window entitled *Schematic#1 MG2A sheet1* will appear.
4. Obtain circuit components from the library with this procedure: Select the LIBRARY icon in the *schematic_add_route* palette. Select *Connectivity Symbols* in the resulting *MGC BPL Libraries* palette. We will select the components to be used in developing the schematic diagram as given on Page 8, and position them approximately at the desired locations. We will subsequently use the MOVE command for final placement.
5. Click on *ground* in the Connectivity Symbols window, and click **OK**. Use the mouse to move the ground symbol into drawing region 3C at the location shown in the diagram. Repeat this procedure to obtain *portin*, and place the resulting input port symbol in region 1A to represent the port labeled A in the diagram. To obtain another portin symbol, click on the symbol in the active symbol window above the palette. Place this port in region 1A at the location designated for input port B on the diagram. Use the same procedures to obtain *portout* and *Vcc* and place the appropriate number of each as shown on the reference diagram:

To obtain the NAND gate symbol, click on *Glue Logic* in the *MGC BPL Libraries* palette. In the resulting *Select Digital Logic* window, for *By Component Name:* type **74LS00**, and click **OK**. Place the NAND gate at an appropriate location on your schematic, and then select and place four more NANDs from the active symbol window. Repeat these procedures for the remaining gates, using the following part numbers:

74LS02 (NOR), 74LS04 (INV), 74LS08 (AND), 74LS32 (OR)

When you have completed your selection of devices, click on ADD/ROUTE at the top of the *MGC BPL Libraries* palette to restore the *schematic_add_route* palette. Note that all of the items placed in the menu remain selected (highlighted). Push the F2 key to unselect them, or use the LMB to choose [schematic_] *UNSELECT ALL*, or do a U stroke with the MMB (start at upper left of U).

6. If you have not placed the required quantity of certain objects, you may use the [schematic_add_route] *COPY* command. This command will make a copy of all items

which are selected, so be sure to use the F2 key to unselect all items before selecting the item(s) to be copied. The [schematic_add_route] *DELETE* command or the Delete key will delete all selected items. Multiple items may be selected by using the LMB to drag a rectangle encompassing the items.

To reposition one or more items on the schematic, select the item(s) and click the LMB on [schematic_] *MOVE*. Note that the MOVE dialog box remains active to allow successive select and move operations. Terminate the operation by clicking on the *Cancel* button in the dialog box, or by pushing the *Esc* key.

7. "Wire" the elements together as shown in the schematic. The wires are connected to the component pins which are displayed as purple diamonds. Click the LMB on [schematic_add_route] *ADD WIRE*. Note that the ADD WI dialog box appears at the bottom of the window, and a white + is attached to the cursor when it is inside the schematic window. Connect the upper input port in region 1A to the upper input of the bottom left 74LS02 NOR gate in region 3C:

You can make a wire connection to another wire by clicking at the intersection point as you draw the wire.

Note that the dialog box at the bottom of the window remains active to allow repeated addition of wires. As with other dialog boxes, it is terminated by clicking on the Cancel button or by pressing the Esc key. Also note that the nets remain selected (highlighted) as they are added.

Draw the remainder of the wires as shown in the schematic diagram. It is a good idea to draw the longest wires first, and then connect the shorter ones from the component pins to the intermediate points on the longer wires.

8. Assign appropriate names to all of the input and output ports, which are initially labeled "NET": Perform *UNSELECT ALL*. Select *TEXT* in the palette, and then select [schematic_text] *CHANGE VALUE*. When the SEL TE dialog box appears, drag the mouse with the LMB to make a rectangle which encloses the NET text on the two input ports. When the CHA PR V dialog box appears, the NET corresponding to input A will be highlighted. Type **A** in the *New Value* box and press Return. The Net Name A will appear on the top input, and the NET corresponding to input B will be highlighted. Type **B** in the *New Value* box and press Return. Repeat this procedure for the leftmost column of four output ports. Continue in this manner until all 14 NETs have been renamed.
9. Check the completed schematic sheet: Invoke pull-down item *Check>Sheet*. A report window will appear, which should indicate 0 Errors and 0 Warnings.
10. Save the completed schematic.
11. Obtain a printed copy of the schematic.
12. Minimize the Design Architect.

b) Simulation with QuickSim II

1. In the Design Manager navigator window, use the RMB to invoke *Update Window* from the pop-up menu. Your MG2A icon should appear in the window. Select the MG2A icon

with the LMB, and then use the RMB to invoke *Open>QuickSim II*.

When the QuickSim II window appears, maximize the window. Click on *OPEN SHEET* in the Setup palette. A window labeled */:sheet1* with your schematic diagram for MG2A should appear.

2. Create a waveform window for all ports in the schematic: Select ports A and B by clicking the LMB on the ports in the schematic window. This actually selects the entire net to which the port is attached, as indicated by the corresponding highlighting. Click the LMB on *TRACE* in the QuickSim palette, and a Trace window will appear, with the port (net) names highlighted to indicate that they are still selected. Select the 12 output ports in the schematic in the order in which they appear from top to bottom on Page 8, and select *TRACE* in the palette to add them to the trace window. You may use the F12 key to toggle the display between schematic and trace windows. Re-size the Trace window as necessary so that all 14 traces are visible.
3. If your traces are out of order, you may move them as follows: Select a trace to be moved by clicking the LMB on its label in the Trace window. (It will become highlighted in both windows). Use the RMB to select *EDIT>MOVE* in the pop-up menu. A set of red axes becomes attached to the mouse pointer, and a dialog box appears at the bottom of the window. Move the cursor to the location desired for the selected trace, and click the LMB to effect the move.
4. Generate the waveforms for inputs A and B: Unselect everything, then select waveform A by clicking the LMB on the */A* label in the Trace window. Select *STIMULUS* from the palette. Select *ADD FORCE* from the resulting Stimulus palette. A dialog box will appear with the Signal name set to */A*. Enter the following values from the keyboard: (you may use the Tab key to progress from one entry to the next)

<i>Value 0</i>	<i>Time 0</i>
<i>Value 1</i>	<i>Time 100</i>
<i>Value 0</i>	<i>Time 300</i>

Click **OK** or press **Return** to terminate the dialog box.

Unselect trace */A* and select */B* by clicking on their labels in the Trace window. Click the LMB on the *ADD FORCES* icon in the QuickSim Palette. Enter the following values:

<i>Value 0</i>	<i>Time 0</i>
<i>Value 1</i>	<i>Time 200</i>

Click **OK** or press **Return** to terminate the dialog box.

5. Run the simulation: Click the LMB on *RUN* in the palette. Click the LMB on *For Time* in the resulting submenu. In the resulting Run Simulation dialog box, enter *For Time 400*, and click **OK**. All of the simulated waveforms should appear in the Trace window. An alternative method for running the simulation is to type **run 400** on the keyboard when the mouse is in the Trace window.
6. If you need to modify your schematic and re-simulate, do NOT exit from QuickSim. Instead, minimize the QuickSim window and its command window, and then double-click the LMB on your *Design_Arch* icon to activate your da schematic. Modify, **check** and **save** your schematic. Double-click on the QuickSim icon to reactivate the simulator. Select

[DESIGN CHG] RELOAD MODEL>All from the palette. The latest version of your schematic will be loaded for simulation. Your forces and the trace window setup will not be affected by this reload, but the simulated time will be reset to zero. Note that this procedure will not work for the invocation of a schematic having a different name.

7. Obtain a printer plot of the waveforms: Click the LMB anywhere in the Trace window to be sure that it is selected (as indicated by the light blue border). Select the pull-down item *File>Print>Active Window*. In the Print Traces dialog box which appears, enter the values for the start and end times of the plot as follows:

Begin Domain 0 End Domain 420

Leave *Scale* blank. Click on the OK box, and the plot will spool to the printer. The final value of 420 nanoseconds is chosen to be slightly larger than the simulation time of 400 ns to assure that the ends of the traces are plotted.

8. To shut down: Select *Quit* from the pull-down menu, and then select *Without Saving* and OK in the dialog window. If you are not going to continue immediately with Part MG2B, then *Quit* Design Architect and *Quit* the two unix windows from which you invoked QuickSim and Design Architect. Finally, *Quit* Design Manager. An improper shutdown may leave **.lck* files in the mentor directories which must be removed with unix commands before you can access the associated files.

Part MG2B. Two-Switch Lamp Control

A lamp is to be controlled by two switches so that any change in the state of either switch (not both) will change the state of the lamp. The state of each device is either "ON" or "OFF". The logic for this switching problem can be satisfied by a single 2-input exclusive OR (XOR) gate. We have seen in class that the XOR function can be realized with a circuit containing four 2-input NAND gates.

For this part of the experiment, you are to follow the same procedure as given in some detail in Part MG2A to create a schematic containing two input ports labeled A and B connected to a single 74LS86A 2-input XOR gate, as well as to a circuit of four 74LS00 2-input NAND gates configured to implement the XOR function. Use label XOR for the output of the 74LS86 gate, and XOR_NAND for the output of the 74LS00 gate which produces the XOR function.

1. Create a schematic called MG2B to satisfy these requirements, and obtain a printer plot.
2. Simulate your circuit with the same forcing waveforms and execution time (400 ns) as in Part MG2A. Arrange waveforms in the Trace window in the following order, from top to bottom: /A, /B, /XOR, /XOR_NAND. Obtain a printer plot of the Trace window.

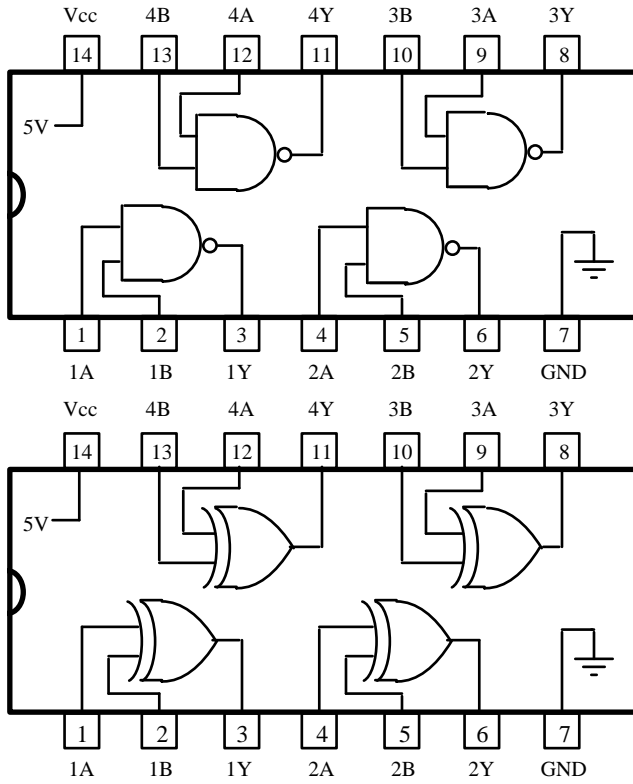
Report

Your report should contain the schematic diagrams and simulation traces for Parts MG2A and MG2B, together with a brief commentary on the lessons learned and problems encountered.

Part HD2 (Second Week)

The purpose of this hardware laboratory is to experimentally verify the operation of the two solutions to the two-way lamp controller which were simulated in Part MG2B of this experiment.

1. Insert a 74LS00 Quad 2-input NAND gate and a 74LS86A Quad 2-input XOR gate into the IDL-800 circuit board. The pin numbering diagrams are shown below on this page.
2. Sketch in your lab notebook the schematic diagrams for your NAND and XOR solutions to the two-way lamp problem from Part MG2B of this experiment. Use switches SW1 and SW0 as the inputs for both circuits. Use LEDs L1 and L0 to display the output of the NAND and XOR circuits, respectively. Draw these connections, as well as all pin assignments on your notebook diagram. Show also the +5V and ground connections with appropriate IC pin numbers.
3. Wire the circuits in accordance with your diagram of Part 2 above.
4. Experimentally determine and record in your notebook the truth table for the outputs L1 and L0 as functions of the switches SW1 and SW0.
5. Design a five-way lamp controller using only 2-input XOR gates, configured for the minimum number of logic levels. Wire your circuit, adding SW4, SW3, and SW2 to your design of Part 2. Put the annotated schematic and truth table in your notebook.
6. How many 74LS00 packages would be required for a five-way NAND realization?



74LS00
Quadruple 2-Input
NAND Gate

74LS86A
Quadruple 2-Input
XOR Gate

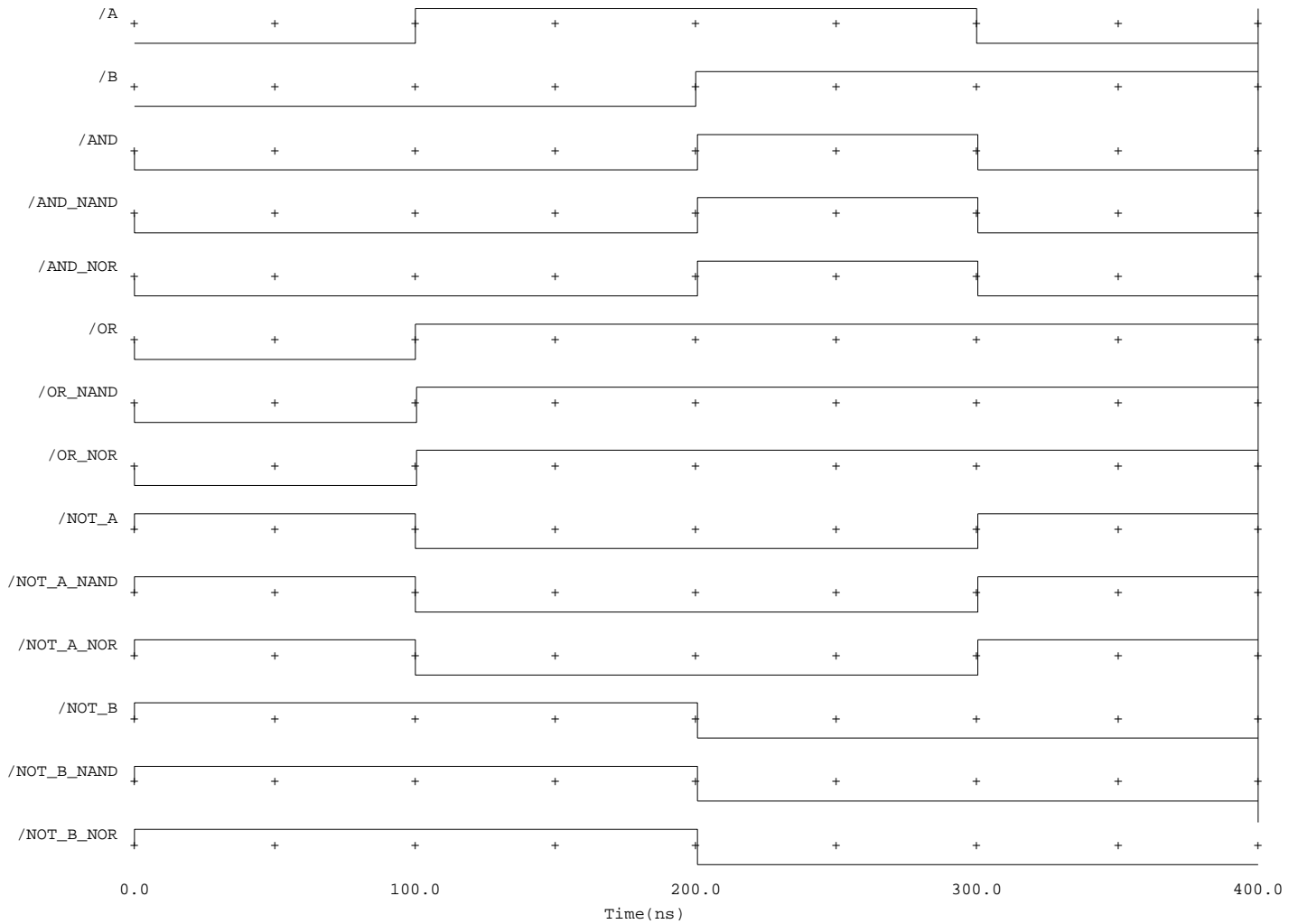
File Name :

Title :

Creator : Mentor Graphics PostScript Filter

CreationDate : Wed Feb 2 15:32:48

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### MG2A QuickSim Traces

These traces were obtained in the default *unit timing mode* which demonstrates the logical behavior of a circuit without showing the actual propagation delays of the components. In later experiments we will invoke the *delay timing mode* to simulate the actual physical behavior of the circuit to include typical propagation delays.