

INTRODUCTION TO THE LOGIC DESIGN HARDWARE LABORATORY

Objectives

This experiment will introduce the features and operation of the IDL-800 Digital Lab unit and the EISTAR Logic Probe, investigate the relationship between logic values 0 and 1 and their corresponding voltage levels in TTL and CMOS technologies, and verify the operation of the SSI (Small-Scale Integration) logic gates AND, OR, and NOT.

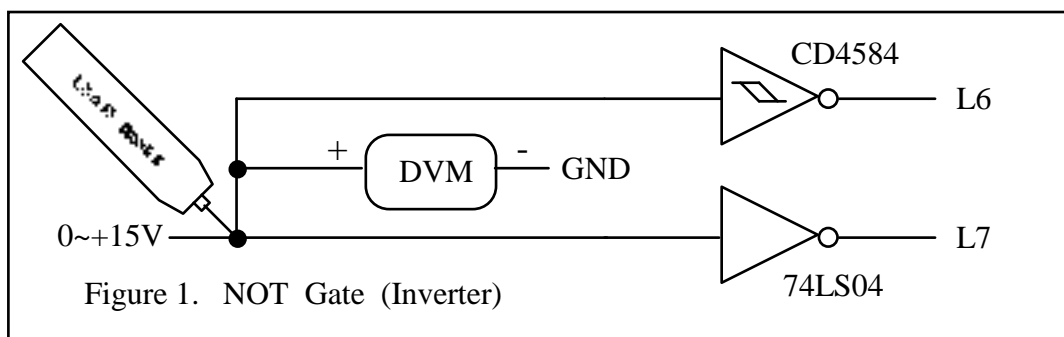
Logic Laboratory Familiarization

1. The instructor will explain the basic features of the IDL-800 Digital Lab unit. A summary description is found on Page 6, and the IDL-800 is shown pictorially on Page 7. A list of the parts in the laboratory kit is given on Page 8.
2. The instructor will explain the function and use of the EISTAR logic probe.

The NOT Gate (Inverter) & Voltage Levels for Logic Values

Logic values of True and False or Boolean algebra values of 1 and 0, which are used in the mathematical analysis of digital logic, are represented as voltage levels in the integrated circuit implementation of physical digital circuits. Here we will experimentally determine voltage levels for TTL Low-Power Schottkey and CMOS devices. See the discussion on *Logic Voltage Ranges* on Page 4 of your textbook (Mano and Kime), and the definition of Noise Margins on Page 3 of this document.

1. Insert a 74LS04 Hex Inverter (six inverter gates in one IC package) into the breadboard with pin 1 at location 1F3 (Row 1, Column F, in the third IC block from the left - beneath L6). Insert a CD4584 (MC14584) Hex Schmitt Trigger Inverter with pin 1 at 10F3. The IC pin configurations are shown on Page 5 of this experiment. Turn off the IDL-800 before wiring.
2. Wire the circuit as shown in Figure 1. Connect +5V to breadboard location 2V1, and GND to the breadboard top row, and wire from those locations to the IC power pins. Connect the red clip of the logic probe cable to +5V, and the black clip to GND. Connect the tip of the logic probe to the 0~+15V supply, and turn the control fully counter-clockwise to zero.



3. For the TTL and CMOS devices we will use in this laboratory, the *nominal* voltages associated with logic zero and logic one are 0 Volts and +5 Volts, respectively. (See page 9 for a brief description on the TTL and CMOS logic families). However, each type of device recognizes a range of **input** voltages between 0 and V_{ILmax} as a logic zero, and a range of **input** voltages between V_{IHmin} and +5 Volts as a logic one. Input voltages between V_{ILmax} and V_{IHmin} produce an invalid or indeterminate logic level.

The logic probe has a switch to select recognition of either TTL or CMOS levels, and it has green and red light-emitting diodes (LEDs) to indicate correspondingly valid inputs of logic zero or logic one, respectively. If neither LED is on, then the voltage is in the invalid range.

Turn the 0~15V control to 0 (fully CCW) and turn on the IDL-800 power. Set the DVM to the 20V range. **Never exceed 5V (control at about 9 o'clock) from the 0~15V supply in this lab.**

4. Use the DVM to measure the actual value of the +5 V supply, and record the value under V_{CC} in the table below, as well as in your notebook.
5. Attach the DVM and the logic probe tip to the output of the 0~+15 V supply, and set the probe switch to TTL. The green LED on the probe should be on (but dimly). Slowly increase the voltage by rotating the control clockwise until the green light goes out. Record the DVM reading for V_{ILmax} in the TTL column below, and in your notebook.
6. Continue slowly rotating the control clockwise until the red light comes on. Record the DVM reading for V_{IHmin} in the TTL column below, and in your notebook.
7. Set the probe switch to CMOS, rotate the voltage control fully CCW, and repeat steps 5 and 6 for the corresponding CMOS measurements.

V_{CC}	Logic Probe	
	TTL	CMOS
V_{ILmax}		
V_{IHmin}		

Now that we have established the valid input voltage ranges for logic zero and logic one as (0 to V_{ILmax}) and (V_{IHmin} to V_{CC}), respectively, we will measure the inverter outputs to verify that their voltages lie within these ranges.

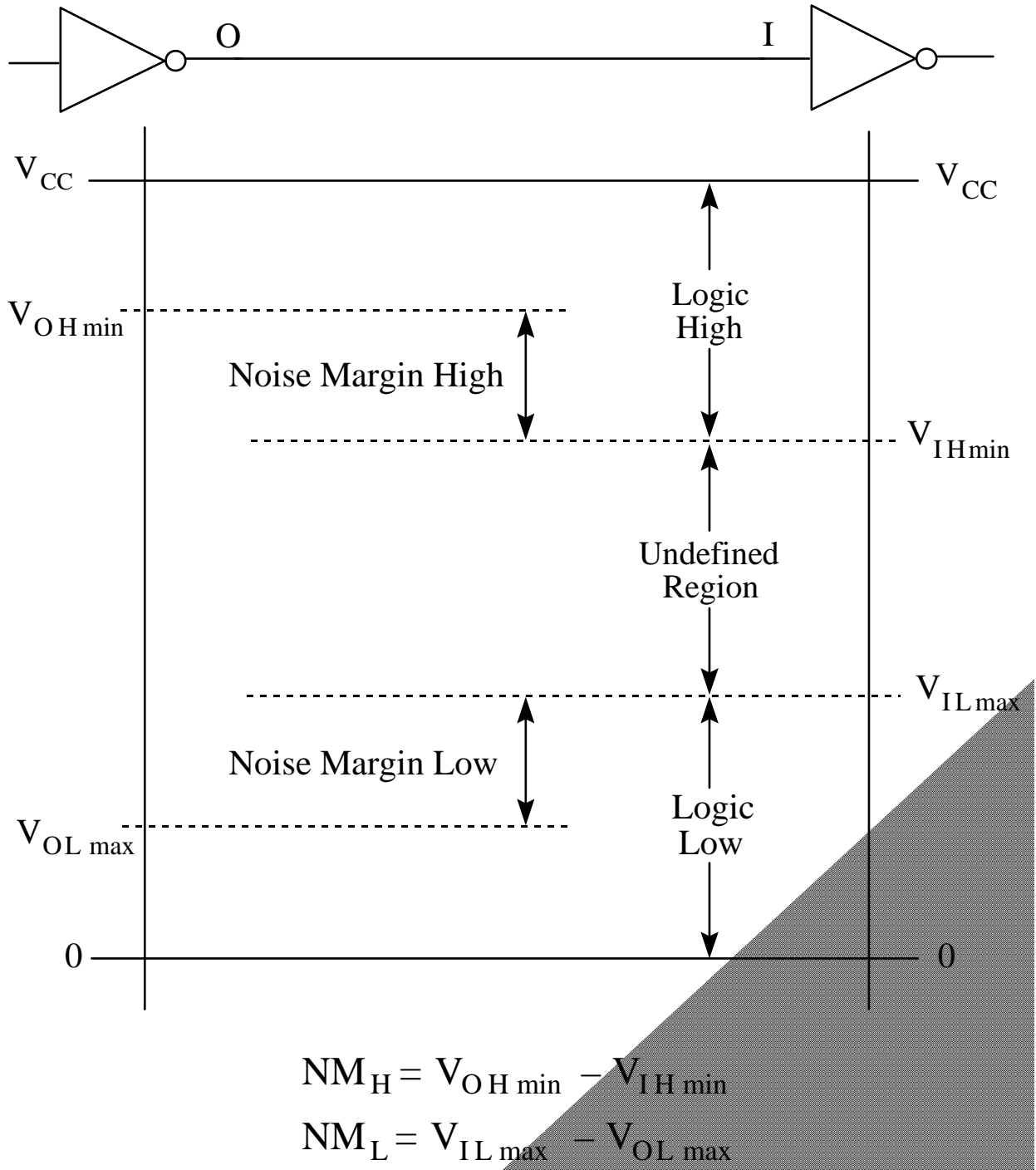
8. Connect the + terminal of the DVM to the output of the 74LS04, which is also connected to L6. Set the voltage control fully CCW so that L6 is on. Record the DVM reading for V_{OHmin} in the LS column below, and in your notebook.
9. Increase the voltage a slightly beyond the point where L6 turns off, and record the DVM reading for V_{OLmax} in the LS column below, and in your notebook.
10. Connect the + terminal of the DVM to the output of the CD4584, which is also connected to L7, and repeat steps 8 and 9 for the corresponding CMOS measurements.

	Inverter	
	74LS04 TTL	CD4584 CMOS
V_{OHmin}		
V_{OLmax}		

Verify for your measurements of both TTL and CMOS that:

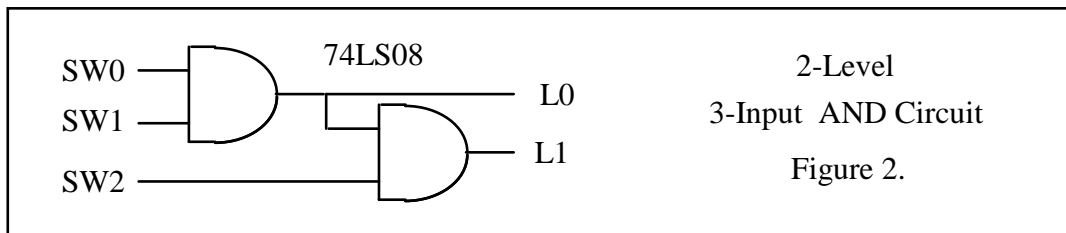
$$V_{OLmax} < V_{ILmax}, \quad \text{and} \quad V_{OHmin} > V_{IHmin}.$$

Noise Margins for Digital Logic



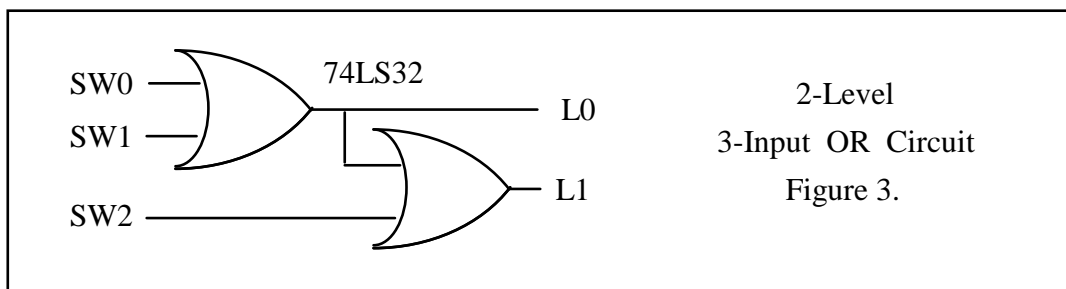
AND Gates

1. Insert a 74LS08 Quad (4 gates in one IC package) 2-input AND gate IC into the breadboard, with pin 1 at location 1F4. Wire the +5V from 2V1 to 2V2.
2. Wire two AND gates from this IC as shown in Figure 2. The pin numbering diagram for the 74LS08 is shown on Page 5 of this experiment. Wire power Vcc and GND.
3. Experimentally verify that this circuit works properly by determining and recording the corresponding truth table. Arrange your column headings as SW2 SW1 SW0 L1 L0. The eight rows should contain the input switch combinations as binary numbers from 0 0 0 to 1 1 1 in a binary counting sequence. The L1 and L0 are 0 if the LED is off and 1 if it is on.



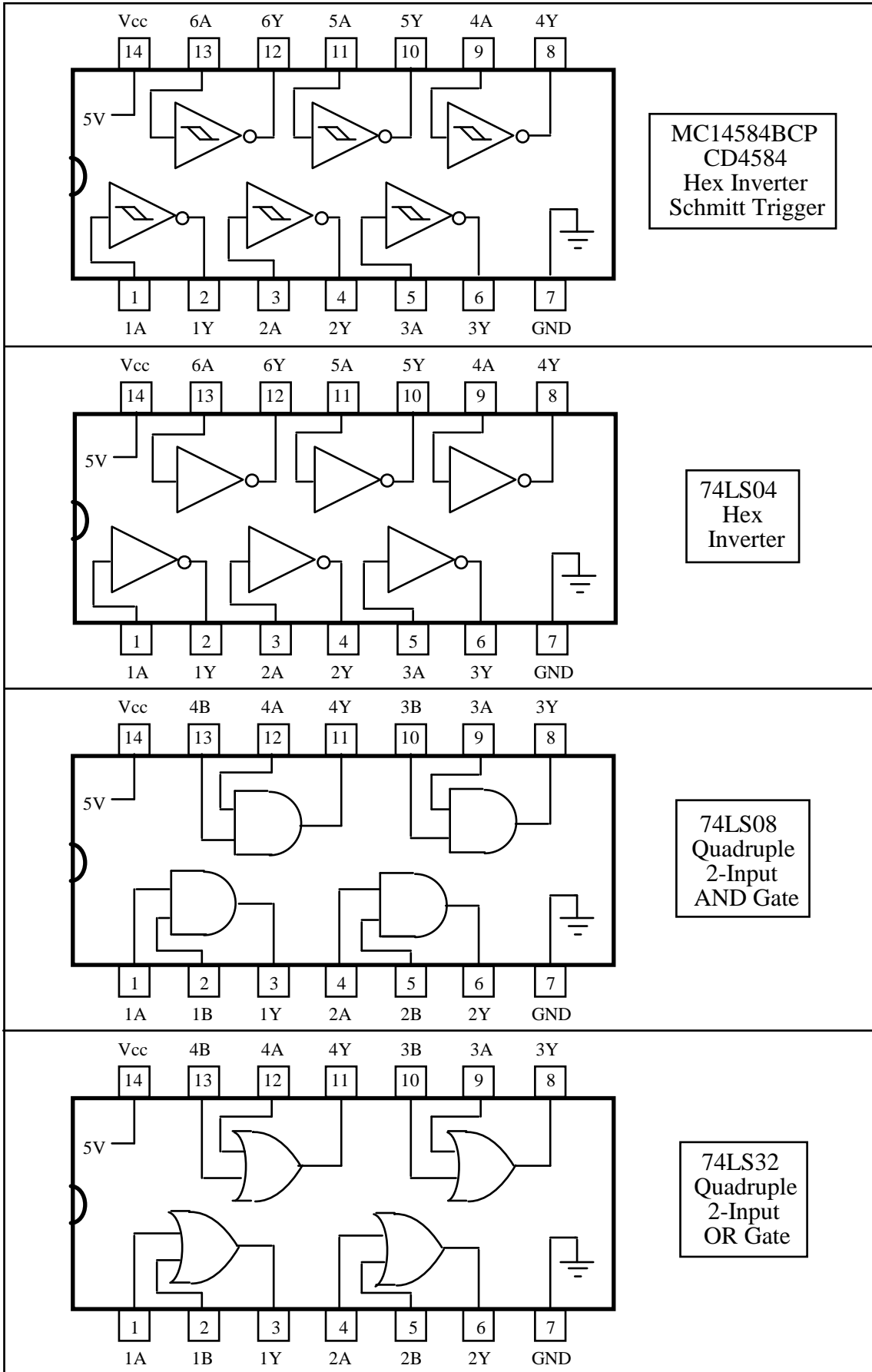
OR Gates

1. Remove the 74LS08 AND IC from the breadboard and insert a 74LS32 Quad 2-input OR gate into the same location. Note that the pin numbering diagrams on Page 5 of this experiment show the same configuration of gates for these two ICs.
2. Without any further wiring, your circuit is now configured as shown in Figure 3 below.
3. Experimentally determine and record the truth table, using the same format as before.



Results

1. Your laboratory notebook should contain:
 - a) The completed tables of voltage measurements from Page 2.
 - b) The AND Gates truth table, and circuit diagram annotated with IC pin numbers.
 - c) The OR Gates truth table, and circuit diagram annotated with IC pin numbers.
 - d) Answers to the following questions.
2. Which technology, TTL or CMOS, has greater noise immunity? Use the data from this experiment to explain your answer.
3. Show how you could construct a 5-input AND circuit with one 74LS08 IC.
4. From your truth tables, explain the physical significance of the terms AND and OR.



The IDL-800 Digital Lab Unit

A pictorial diagram of the IDL-800 Digital Lab Unit is shown on the next page. The *Power Switch* is located in the upper left corner. This switch should be OFF while you are inserting components and wires into the breadboard.

To the right and below the power switch is a *Function Generator* which produces a periodic selectable sine, triangle or square waveform with adjustable amplitude from 0 to 7 Volts peak-to-peak, and adjustable frequency from 1 Hz to 100 KHz. The signal is capacitively coupled to the OUT terminal, so it is not directly suitable as a clock input for digital logic circuits. However, a good *Digital Clock* signal can be obtained from the output of a 74LS04 inverter whose input is connected to OUT on the Function Generator *after* selecting a Square waveform and setting the Amplitude at 10 o'clock as shown in the diagram.

To the right of the Function Generator is a *Digital Voltmeter* (DVM). The full-scale range is manually selectable between 200 millivolts and 200 Volts. Set the range to 20 Volts for this lab.

A *Binary-Coded-Decimal to 7-Segment Decoder* and two *7-segment Light-Emitting Diode Displays* are located directly below the Function Generator. An 8-pole DIP switch allows connection of the individual decoder outputs to the LED segments on the two displays. The BCD code is connected to the four inputs D, C, B, A, where A is the least significant bit. The common-cathode connection D1 or D2 must be connected to GND to activate the corresponding display.

L0 through L8 are unlatched LED displays which turn on whenever a logic 1 (between 3 and 5 Volts) is applied at the input connection.

SW0 through SW7 are independent slide-switches which can be set to maintain an output of either logic 0 (0 Volts) or 1 (5 Volts). The output is undefined when the switch is changed from one position to the other. These outputs should not be used to clock edge-triggered flip-flops.

Pulse Switches A and B are independent spring-loaded push-button switches with associated complementary flip-flop outputs. These are "debounced" outputs which may be used to trigger flip-flops. The "Pulse" begins when the button is depressed and ends when it is released.

Power connections are available on the left side of the unit. Two connection blocks provide VCC = +5V for digital ICs, and three blocks on the left as well as one on the right provide the ground (GND). Be sure to observe the proper polarity in your connections to the IC chips. There is one connection block for a fixed -5V. SWA and SWB are three-position slide switches which allow selection of fixed voltages of -5, 0 and +5. Continuously variable supplies for 0 to +15V and 0 to -15V are also located on the left side of the unit.

External connections are available for banana plugs through Adapters 1 and 2, and for BNC cables through Adapters 3 and 4.

The removable *breadboard* consists of two identical units, each of which can accommodate two columns of IC Dual-In-Line (DIP) packages. The DIPs are inserted in a vertical orientation with the left column of pins in column F, and the right column of pins in column G. In each of the rows numbered from 1 to 28, there are four independent instances where the six connections ABCDEF are common (electrically connected), and where the six connections GHIJKL are common. At the bottom of the breadboard, in each column numbered 1 to 30, the connections abcdef are common. The 24 connections in the top row of each of the two breadboard units are common, as are the 24 in row below V3-V4. These 96 connections are intended for power GND.

The 12 connections at each V1, V2, V3, V4 site are common, but independent of the other sites. The V sites are intended for power VCC with digital logic, and for other positive or negative power voltages with memory or analog ICs.

CSE 221L Logic Design Laboratory

Component Kit

Row, Col	Qty	Part No.	Description
	1	WK-1	Wire Kit
(1, 1) (1, 2)	2	74LS00	Quad 2-input NAND Gate
(1, 3)	1	74LS02	Quad 2-input NOR Gate
(2, 1)	1	74LS04	Hex Inverter
(2, 2)	1	74LS08	Quad 2-input AND Gate
(2, 3)	1	74LS10	Triple 3-input NAND Gate
(3, 1)	1	74LS20	Dual 4-input NAND Gate
(3, 2)	1	74LS32	Quad 2-input OR Gate
(3, 3)	1	74LS74A	Dual D Flip-Flop
(4, 1) (4, 2)	2	74LS76A	Dual JK Flip-Flop, Clear, Preset
(4, 3)	1	74LS86	Quad 2-input XOR Gate
(5, 1)	1	74LS138	1 of 8 Decoder
(5, 2)	1	74LS153	Dual 4-input Multiplexer
(5, 3)	1	74LS157	Quad 2-input Multiplexer Noninv
(6, 1) (6, 2)	2	74LS169	4-bit Binary Up/Down Counter
(6, 3)	1	74LS175	Quad D Flip-Flop with Clear
(7, 1)	1	74LS194A	4-bit Right/Left Shift Register
(7, 2)	1	74LS390	Dual Decade Counter
(7, 3)	1	CD4584	CMOS Hex Schmitt Trigger MC14584
	1	RA10K	Resistor 10K, 1/4 W. Brwn, Blk, Orng
	1	RA68K	Resistor 68K, 1/4 W. Blue, Gray, Orng

The Row and Column entries in the first column of this table are the suggested storage locations of the 21 ICs when they are laid out horizontally in a 7 by 3 matrix, to provide rapid identification.

Logic Families*

Electronics provide several different types of technologies and design techniques that can be used to build digital logic circuits. This is accomplished by starting with a simple logic gate, such as a NOT or an AND, that is built from transistors that are used as electronic switches. Once a basic gate is created, it may be possible to use the same ideas to create other useful logic gates. The logic gates that are created using the same basic circuit design are known as a **logic family**. Gates that belong to a particular logic family are similar in parameters such as power supply value, output voltage levels, propagation delay times, and other characteristics. This similarity allows for easy interfacing for building large systems.

Next, two logic families that are most commonly used to build digital systems are described.

CMOS

CMOS is an acronym that stands for **Complementary Metal Oxide Semiconductor**. This is a type of technology that allows for extremely high-density integrated circuits and forms the basis of modern chip design. The transistors used to create the switching circuits in **CMOS** are called **MOSFETs** (**MOS Field-Effect Transistors**). MOSFETs can be made extremely small: devices smaller than about $0.3 \mu\text{m} \times 1 \mu\text{m}$ are typical. Since the transistors are so small, several million individual devices can be created on a single “chip” of silicon that is only 1 or 2 cm on a side. This allows for a complex digital networks, such as microcomputers, to be integrated into a single low-cost unit.

Some of the important characteristics of CMOS are summarized below.

Power Supply: CMOS integrated circuits commonly use a power supply value of $V_{DD} = 5$ volts. However, some CMOS chips can operate over a range of values (typically 5 v to 15 v), and more advanced designs use 3.3 v and lower. A small power supply voltage is advantageous for reducing the power consumption and hence the heating. In addition, it makes battery-operated systems more practical.

Logic Levels: One advantage of CMOS is that it provides output logic voltages that range from 0 v to the value of the power supply V_{DD} . This provides ideal voltage levels for logic 0 and logic 1 states.

Propagation Delay: The propagation delay t_p through a simple inverter (NOT) circuit is on the order of 0.1 nanoseconds or smaller if measured inside the integrated circuit. More complex logic networks have propagation delays of several nanoseconds.

TTL Integrated Circuits

TTL (**Transistor-Transistor Logic**) is another popular logic gate family. In the early days of microcomputing, TTL chips were used almost exclusively to provide “glue logic” that allowed various chips in the computer to communicate with each other.

TTL is based on a different type of transistor from those used in CMOS chips. These devices, known as bipolar transistors, can be used to design very fast switching networks. However, bipolar transistors are much larger than MOSFETs, they are more difficult to connect together, and bipolar circuits can exhibit extreme heating problems. Owing to these considerations, they are not usually the first choice for high-density chip designs. However, bipolar logic circuits and TTL ICs are still important in hundreds of applications, because they provide reliable, low-cost logic chips that are easy to use.

Power Supply: TTL integrated circuits are designed for a power supply voltage of $V_{DD} = 5$ volts only. If a different value is used, then the circuit will not operate properly and may be destroyed.

Logic Levels: Even though TTL circuits use a power supply voltage of $V_{DD} = 5$ v, the output levels measured from a typical gate cannot attain this level. Typically, $V \approx 0.3$ v is the lowest value of the output voltage, and $V \approx 3.6$ v is the highest value. This reduced logic swing is due to electrical characteristics of the bipolar transistors. In general, the reduced logic voltage range is not a problem if TTL is used throughout the design.

Propagation Delay: Bipolar transistors can be switched very quickly. A TTL integrated circuit usually has propagation delays on the order of a few nanoseconds as measured outside the circuit package.

* Adopted from J. P. Uyemura, “*A First Course in Digital Systems Design: An Integrated Approach*”