

CSE 563

Advanced VLSI

7/20/95

Spring Semester of odd-numbered years

CSE 563: "Advanced VLSI" (3-0-3)

An introduction to most aspects of large-scale, handcrafted CMOS integrated circuit design including: device fabrication; artwork rules; useful circuit building blocks; and system design and layout considerations. System design considerations will include power supply level fluctuations, high-speed clocking methods, estimating interconnection delay, and design for testability. Chip system floorplanning will also be treated in depth. All circuits and systems will be digital and will be considered in the context of CMOS technology. Homework will require the use of existing Mentor IC mask artwork software.

Texts: M. Shoji, *CMOS Digital Circuit Technology*, Prentice-Hall, 1988.
H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley, 1990.

Professor-in-Charge: S.C. Bass

Course Goals:

To impart a thorough understanding of the *system* aspects of the handcrafted CMOS VLSI design of large structures.

Prerequisites:

- a. Courses: CSE 462 or similar introductory VLSI course.
- b. Topics: Experience with the Mentor Graphics design tools *Design Architect* and *QuickSim*.

Topics:

Number of Lectures:

Review of NAND'S, NOR's, and other basic CMOS gates	1/2
Review of basic MOS device operation and square-law models	1 1/2
Inverter logic threshold formula	1/2
CMOS fabrication steps	2
Artwork rules: Origins and usage	1 1/2
Gate, diffusion, and wiring capacitances	1/2
Charge storage: Uses and pitfalls	1/2
Static and dynamic latches and shift registers	1
Full adder circuits	1/2
Implementing databuses	1/2
Dynamic gating; Domino and NORA logic	2
PLA design and layout; finite-state machines	1
Transistor sizing; minimizing delays through inverter chains	1-1/2
Driving long transmission gate chains	1-1/2
Driving long interconnect lines	1/2
Pad drivers and receivers	1 1/2

Latch-up mechanism	1
Metastable states in latches	1-1/2
Power and ground routing	1-1/2
Power supply fluctuations	1-1/2
Exam	1-1/2
Estimating and modeling on-chip wiring delays	1-1/2
Gunning Transceiver Logic (GTL) interface circuit for high-speed off-chip communications	1
High-speed clocking techniques	6-1/2
Design for testability: Level-Sensitive Scan Design and Signature Analysis	3
Classic process scaling effects	1
Procedures for orderly floorplanning of large IC systems	4
Additional topics, time permitting	1
Mid-term examination	1

Computer Usage:

Extensive use of the Mentor Graphics digital system design tools as installed on Sun SPARC workstations.

Laboratory Usage: None

References: N. Weste and K. Eshraghian, *Principles of CMOS, VLSI Design: A Systems Perspective, 2nd Ed.*, Addison-Wesley, 1993.

Grading:

Homework	25%
Mid-term	35%
Project	40%

Special Considerations: None

Course Content:

Engineering Science:	1.0 credit
Engineering Design:	2.0 credits

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