In this PLA design, one approach is to:
- Bring in the x and S data (from bottom-to-top)...
- ...and then clock from left-to-right.
In this PLA design, we preprogram.

- Programming / select signals can be brought into the design from the top right. We can force a 0 at the right end of the \( f \) lines. In this way, the select signal will enter a node, the AND gate will act as a majority gate with 2 0s – and hence a 0 will come out, and the output of the OR gate into the (yellow) “latch” will be the select signal value – as both inputs to the OR gate are separate. Hence, the select signal will determine the output. The yellow latches will be kept high – keeping the programming signal latched.

- A computation will proceed from the bottom left to top right. Everything could be done in one time step/clock zone, or data could be pipelined. The clock wave form will also progress from bottom left to top right in a wave like fashion. If data is pipelined, two \( f \) values will be output every cycle. Thus, a “CPI” will be 2.
PLA Design #3:

```
| S_A-3 |  | S_B-3 |  | S_C-2 |  |
|-------|  |-------|  |-------|  |
| S_B-2 |  | S_B-2 |  | S_C-2 |  |
|-------|  |-------|  |-------|  |
| S_A-2 |  | S_B-1 |  | S_C-1 |  |
```

```
X
---
f_3
X
---
f_2
X
---
f_1
X
---
f_0
X
---
```

```
| S_A |  | S_B |  | S_C |  |
|-----|  |-----|  |-----|  |
| x_0 |  | x_0' |  | x_1 |  |
| x_0 |  | x_0' |  | x_1 |  |
| x_0 |  | x_0' |  | x_1 |  |
| x_0 |  | x_0' |  | x_1 |  |
```
In this design, data and select signals “counterflow” – similar to Sutherland’s work. Also, f signals still flow from left to right – and data flows up and to the right in a wave like fashion. Some signals have been started in the various “pipelines”.